DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **Capacitors, DRAM Arrays, Monolithic Integrated Circuits, And Methods Of Forming Capacitors, DRAM Arrays, And Monolithic Integrated Circuits**, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

POWER OF ATTORNEY:

As a named Inventor, I hereby appoint the following attorneys and agent to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Richard J. St. John, Reg. No. 19,363; David P. Roberts, Reg. No. 23,032; Randy A. Gregory,

Reg. No. 30,386; Mark S. Matkin, Reg. No. 32,268; James L. Price, Reg. No. 27,376; Deepak Malhotra, Reg. No. 33,560; Mark W. Hendricksen, Reg. No. 32,356; David G. Latwesen, Reg. No. 38,533; George G. Grigel, Reg. No. 31,166; Keith D. Grzelak, Reg. No. 37,144; John S. Reid, Reg. No. 36,369; Lance R. Sadler, Reg. No. 38,605; James D. Shaurette, Reg. No. 39,833; Lia Pappas Dennison, Reg. No. 34,095; and Michael L. Lynch, Reg. No. 30,871.

Send correspondence to: WELLS, ST. JOHN, ROBERTS, GREGORY & MATKIN P.S., 601 W. First Avenue, Suite 1300, Spokane, WA 99204-0317. Direct telephone calls to: David G. Latwesen, Ph.D. (509) 624-4276.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * * *

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/765,510
Priority Filing Date . . . . . January 19, 2001
Inventor . . . . . Kunal R. Parekh et al.
Assignee . . . . . Micron Technology, Inc.
Priority Group Art Unit 2813
Priority Examiner . . . . . Y. Huynh
Attorney's Docket No. MI22-1816
Title: Capacitors, DRAM Arrays, Monolithic Integrated Circuits, And Methods of Forming Capacitors, DRAM Arrays, And Monolithic Integrated Circuits

Assistant Commissioner for Patents
Washington, D.C. 20231

ASSOCIATE POWER OF ATTORNEY

Please recognize Frederick M. Fliegel, Reg. No. 36,138; D. Brent Kenady, Reg. No. 40,045; James E. Lake, Reg. No. 44,854; Bernard Berman, Reg. No. 37,279; and Jennifer Taylor, Reg. No. P-48,711; whose post office address is 601 W. First Avenue, Suite 1300, Spokane, Washington 99201-3828, as associate attorneys or agents in the above-entitled application.

Date: 7/11/01

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